REMARKS

The application has been reviewed in light of the Office Action dated March 6, 2006. Claims 1-20 were pending. By this Amendment, claims 1 and 10 have been amended to clarify the claimed invention. Accordingly, claims 1-20 are now pending, with claims 1, 10 and 19 being in independent form.

Claims 1 and 10 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by U.S. Patent No. 5,758,191 to Kasebayashi et al. Claims 2, 3, 9, 11, 12 and 18 were rejected under 35 U.S.C. § 103(a) as purportedly obvious over Kasebayashi in view of U.S. Patent No. 6,799,242 to Tsuda et al. Claims 4-6 and 13-15 were rejected under 35 U.S.C. § 103(a) as purportedly obvious over Kasebayashi in view of Tsuda and further in view of U.S. Patent No. 6,470,439 to Yamada et al. Claims 7, 8, 16, 17, 19 and 20 were rejected under 35 U.S.C. § 103(a) as purportedly obvious over Kasebayashi in view of Tsuda and Yamada and further in view of U.S. Patent No. 6,502,159 to Chuang et al.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1, 10 and 19 are patentable over the cited art, for at least the following reasons.

This application relates to improvements to communications interfacing techniques which can be used, for example, in an optical disk drive mechanism for communications interfacing between the optical disk drive mechanism and a host computer connected thereto, and can effectively reducing power consumption of an optical disk drive mechanism.

For example, an improved communications interface technique can include storing in a register circuit data to be transferred to a host computer, storing in a first memory first information indicating a specific address of the register circuit and representing an access to a

communications interface apparatus executed by the host computer for a data transfer, storing in a second memory second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and performing an information writing operation with a control circuit for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed. Each of independent claims 1 and 10 addresses these features, as well as additional features. Such features allow the operation mode of the communications interface apparatus to change from low power consumption mode to regular operation mode.

Kasebayashi, as understood by Applicant, proposes an approach for buffer management in the transfer of data between a magnetic disc apparatus and a host system. Fig. 3 of Kasebayashi shows a block diagram of functions of a magnetic disc apparatus proposed by Kasebayashi. Kasebayashi is neither concerned with power management nor with communications interfacing between an optical disk drive mechanism and a host computer connected thereto.

Kasebayashi, column 6, lines 1-13, which is cited in the Office Action, proposes a method of processing data sent from the host computer, and does not disclose any methodology for the handling of data to be transferred to the host computer, as provided by the claimed invention of independent claims 1 and 10 of the present application.

In addition, Kasebayashi does not disclose or suggest the optical disk drive apparatus of claim 19. As mentioned above, Kasebayashi is directed to buffer management in the transfer of data between a magnetic disc apparatus and a host system, and is not concerned with communications interfacing between an optical disk drive mechanism and a host computer

connected thereto.

Claim 19 of the present application is directed to an optical disk drive apparatus comprising an optical disk drive mechanism and an interface circuit. The interface circuit interfaces communications between the optical disk drive mechanism and a host computer, and comprises an input terminal, a data processor, a clock generator, an operation mode changer and a buffering circuit block. The input terminal receives data sent from the host computer. The data processor is configured to perform a predetermined data processing operation to the data received through the input terminal from the host computer. The operation mode changer is configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode. The buffering circuit block is configured to buffer the data received through the input terminal from the host computer. The buffering circuit block includes a first data transfer path, a second data transfer path and a path selection controller. The first data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor not via a memory. The second data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor via a memory. The path selection controller controls the buffering circuit clock to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode.

Tsuda, as understood by Applicant, proposes an optical disc player having a sleep mode. Tsuda proposes that data is supplied from the optical disc player through the host interface to the host computer.

As previously discussed of record, Tsuda is concerned with reproduction of data from an

optical disc, and not with recording of data to the optical disc.

Applicant does not find teaching or suggestion in Tsuda of an optical disk drive apparatus wherein data sent from the host computer is received by the optical disk drive apparatus through an input terminal of an interface circuit of the optical disk drive apparatus, or that such data is processed by a data processor, or that such data is buffered by a buffering circuit, as provided by independent claim 19 of the present application.

Further it is noted that claim 19 would not have been obvious from a combination of Kasebayashi and Tsuda, since Kasebayashi is not concerned with communications interfacing between an optical disk drive mechanism and a host computer and Tsuda is not concerned with data transfer from the host computer to the optical disk drive apparatus.

In addition, Applicant does not find teaching or suggestion in Tsuda of storing in a register circuit data to be transferred to a host computer, storing in a first memory first information indicating a specific address of the register circuit and representing an access to a communications interface apparatus executed by the host computer for a data transfer, storing in a second memory second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and performing an information writing operation with a control circuit for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, as provided by each of independent claims 1 and 10 of the present application.

Yamada, as understood by Applicant, is directed to a FIFO (first-in-first-out) memory control circuit, such as used in an electronic device, for performing asynchronous read/write

control when a write clock and a read clock are different. Yamada was cited in the Office Action as purportedly proposing that the FIFO memory includes a specific number of buffer areas into which data from a host computer is written.

Amongst other deficiencies, Yamada does not disclose or suggest communication of data between the electronic device and a host computer. Therefore, the claimed invention of the present application would not have been obvious from Yamada, alone or in combination with Kasebayashi and Tsuda.

Chuang, as understood by Applicant, proposes techniques directed to improving data throughput in a computer system. Chuang proposes control circuitry responsive to signals from a CPU which specify whether data from a CD-ROM is to be sent directly to a MPEG decoder circuit or to be sent to system memory.

Applicant simply does not find disclosure or suggestion in the cited art, however, of storing in a register circuit data to be transferred to a host computer, storing in a first memory first information indicating a specific address of the register circuit and representing an access to a communications interface apparatus executed by the host computer for a data transfer, storing in a second memory second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and performing an information writing operation with a control circuit for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, as provided by each of independent claims 1 and 10 of the present application.

In addition, Applicant does not find teaching or suggestion in the cited art of an optical

disk drive apparatus comprising an interface circuit which interfaces communications between an optical disk drive mechanism and a host computer, and comprises an input terminal, a data processor, a clock generator, an operation mode changer and a buffering circuit block, wherein the input terminal receives data sent from the host computer, the data processor performs a predetermined data processing operation to the data received through the input terminal from the host computer, the operation mode changer controls the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode, the buffering circuit block buffer the data received through the input terminal from the host computer and includes a first data transfer path, a second data transfer path and a path selection controller, the first data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor not via a memory, the second data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor via a memory, and the path selection controller controls the buffering circuit clock to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode, as provided by claim 19 of the present application.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1, 10 and 19, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any fees that are required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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